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09/874,032	06/06/2001	Jaroslav Hynecek	ISE107	7598

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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 07/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/874,032	HYNECEK, JAROSLAV	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence(s) of the specification or in an application data sheet by identifying the prior application by application number (37 CFR 1.78(a)(2) and (a)(5)).

When the nonprovisional application is entitled to an earlier U.S. effective filling date of one or more provisional application under 35 U.S.C. 119(e), a statement such as "This application claims the benefit of U.S. Provisional Application No. 06/245,942, filed 11/06/2000." should appear as the first sentence of the description or in an application data sheet.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "**210**" (Fig. 2) has been used to designate both upper and lower portions of a transistor. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1 & 7 are objected to because each of these claims recites, "said transistor having a gate surrounding its source and connected to it" which should be changed to --said *vertical punch-through* transistor having *the* gate surrounding *the* source and connected to *the* source-- for proper antecedent basis.

Claims 2, 3, 8 & 9 are also objected to because each of these claims recites, "the vertical charge-sensing punch-through transistor." The "charge-sensing" should be removed for proper antecedent basis.

Claims 10-12 are also objected to because each of these claims recites, "the charge reset means" which is ONLY supported by claim 9, not claim 8. The Examiner suggests the Applicant to change dependency of each of claims 10-12 from claim 8 to claim 9 for proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 7-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in

the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding independent claim 7, the claim recites "a CCD and CMOS device" which is not described in the specification as *a single device*.

Regarding claims 8-12, these claims are rejected as being dependent of claim 7.

The following rejection(s) applied to claims 7-12 based on best understood (by assuming BCD is a CCD and CMOS device) in view of the 112 first paragraph rejection above.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 4 & 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Each of claims 4 & 10 recites, "a standard reset gate." Since "standard" can change over time, the metes and bounds of the claim cannot be ideally ascertained.

The following rejection(s) applied to claims 4 & 10 based on best understood in view of the 112 second paragraph rejection above.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of U. S. Patent No. 6,580,106 B2 (hereafter, referred as Patent '106). Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of the instant application is encompassed by claims 1 & 3 of the Patent '106. It should be noted that "a drain" as claimed in the instant application is inherently met by the claimed vertical punch through transistor in the Patent '106 because a drain must exist as a fundamental terminal in addition to a source and gate of the claimed transistor in order for the transistor to function.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

7. Claim 7 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of the Patent '106 in view of the Admitted Prior Art. *Note an assumption for a CCD and CMOS device mentioned in section 4 above.*

Regarding claim 7, the Patent '106 claims in claims 1 & 3 an image sensor device comprising CMOS and having all features as claimed in claim 7 of the instant application. The claims 1 & 3 of the Patent '106 do not include a CCD. However, as admitted by the Applicant in Fig. 1 and pages 6-8 of the specification that the CCD and CMOS device is a well-known imaging device having a typical BCD structure which comprises a substrate (105) and a gate (104) surrounding its source (109).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the CMOS device in the Patent '106 to include a CCD structure in an alternative implementation of an imaging device based on a well-known BCD structure.

8. Claim 2 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of the Patent '106 in view of Kubo Kazuya (JP 61-188965).

Regarding claim 2, the claimed invention of Patent '106 *does not clearly* disclose a charge present under the gate modulates the punch through potential barrier of the vertical charge-sensing punch-through transistor. It is taught by Kubo that a barrier height of a vertical punch through transistor (Fig. 1) is modulated by the charges present under the gate (4, 7) to

implant excess charge into substrate 1 for suppressing a blooming, expanding a dynamic range and improving the S/N ratio. See Abstract and Fig. 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of modulating the punch through potential barrier of the vertical charge-sensing punch-through transistor by a charge present under the gate for suppressing a blooming, expanding a dynamic range and improving the S/N ratio.

9. Claims 3, 5, 6, 8, 9, 11 & 12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of the Patent '106 and the Admitted Prior Art and in further view of Kubo Kazuya (JP 61-188965).

Regarding claim 8, the claimed invention of Patent '106 and the Admitted Prior Art do not clearly disclose a charge present under the gate modulates the punch through potential barrier of the vertical charge-sensing punch-through transistor. It is taught by Kubo that a barrier height of a vertical punch through transistor (Fig. 1) is modulated by the charges present under the gate (4, 7) to implant excess charge into substrate 1 for suppressing a blooming, expanding a dynamic range and improving the S/N ratio. See Abstract and Fig. 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of modulating the punch through potential barrier of the vertical charge-sensing punch-through transistor by a charge present under the gate for suppressing a blooming, expanding a dynamic range and improving the S/N ratio.

Regarding claims 3 & 9, the Admitted Prior Art further shows a charge reset means (111, Fig. 1) adjacent to and coupled to the vertical charge-sensing punch-through transistor (it is noted that the transistor originates from the Patent '106) to remove charge therefrom (see first paragraph on page 8 of the specification).

Regarding claims 5 & 11, the Admitted Prior Art further discloses that the charge reset means (111) is a resistive reset gate (see first paragraph on page 8 of the specification).

Regarding claims 6 & 12, the Applicant further admits that the resistive reset gate and a lateral punch-through reset gate are obvious variants over each other as well known in the art (see first paragraph on page 10 of the specification). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the charge reset means by using either a resistive gate or a lateral punch through transistor as an alternative over each other.

10. Claims 4 & 10 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of the Patent '106 and the Admitted Prior Art and in further view of Lee et al (US 5,904,493). *Note "best understood" mentioned in section 5 above.*

Regarding claims 4 & 10, the claimed invention of Patent '106 and the Admitted Prior Art do not explicitly teach that the charge reset means is a standard reset gate. Lee teaches that it

is a design choice for a reset means to be constructed with a standard reset gate (using standard CMOS voltage level) or other reset gates using higher voltage level in a combined CCD and CMOS imaging device (see Lee, col. 3, line 65 – col. 4, line 9).

Therefore, it would have been obvious to one of ordinary skill in the art to construct the charge reset means by using a standard reset gate as one of design choices for the charge reset means.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-3, 5-9, 11 & 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art in view of Kubo Kazuya (JP 61-188965).

Regarding claim 1, the Admitted Prior Art (Fig. 1) discloses a charge detection device for use in an image sensor, the charge detection device including a transistor (at Vs, Fig. 1) having a source (109), drain (108, 111) and gate (104), said transistor having the gate surrounding the source and connected to it (see the paragraph starting from page 6 to page 8 of the specification). It is noted that "connected" is considered as physically connected, not necessary to be electrically connected.

The Admitted Prior Art does not teach that the transistor is a vertical punch-through transistor. However, as taught by Kubo, a vertical punch-through occurs between the source region 3 and substrate 1 of a transistor so that excess charges are implanted into the substrate 1 to suppress a blooming, to expand a dynamic range and to improve S/N ratio by removing excess charges after photoelectric converting (see Abstract and Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art to modify the Admitted Prior Art to include the teaching of Kubo for a vertical punch-through transistor so as to suppress a blooming, to expand a dynamic range and to improve S/N ratio by removing excess charges after photoelectric converting, thereby the image quality would be improved.

Regarding claim 2, it is clear from Kubo's teaching that the barrier height of the vertical punch through transistor (Fig. 1) is modulated by the charges present under the gate (4, 7). See Abstract.

Regarding claim 3, it is further disclosed by Admitted Prior Art that a charge reset means (111, Fig. 1) adjacent to and coupled to the vertical charge-sensing punch-through transistor to remove charge therefrom (see first paragraph on page 8 of the specification).

Regarding claim 5, the Admitted Prior Art discloses that the charge reset means (111) is a resistive reset gate (see first paragraph on page 8 of the specification).

Regarding claim 6, the Applicant further admits that the resistive reset gate and a lateral punch-through reset gate are obvious variants over each other as well known in the art (see first paragraph on page 10 of the specification). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the charge reset means by using either a resistive gate or a lateral punch through transistor as an alternative over each other.

Regarding claim 7, see the analysis of claim 1 in section 10. The Admitted Prior Art discloses an imaging device in form of a BCD structure that is also a CCD and CMOS device (see Fig. 1 and pages 6-8 in the specification).

Regarding claims 8 & 9, see the analyses of claims 2 & 3, respectively, in section 11.

Regarding claims 11 & 12, see the analyses of claims 5 & 6, respectively, in section 11.

12. Claims 4 & 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art and Kubo Kazuya as applied to claims 1 & 7 and in further view of Lee et al (US 5,904,493).

Regarding claims 4 & 10, the Admitted Prior Art and Kubo do not explicitly teach that the charge reset means is a standard reset gate. Lee teaches that it is a design choice for a reset means to be constructed with a standard reset gate (using standard CMOS voltage level) or other

reset gates using higher voltage level in a combined CCD and CMOS imaging device (see Lee, col. 3, line 65 – col. 4, line 9).

Therefore, it would have been obvious to one of ordinary skill in the art to construct the charge reset means by using a standard reset gate as one of design choices for the charge reset means.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

DAVID L. OMETZ
PRIMARY EXAMINER